# DESIGNING OF SOME ALL-OPTICAL CIRCUITS FOR QUATERNARY LOGIC BASED DATA AND SIGNAL PROCESSING

*Thesis submitted to*

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# Thesis Certificate

This is to certify that the thesis entitled “Designing of some all-optical circuits for quaternary logic based data and signal processing”, submitted by Tanay Chattopadhyay to the West Bengal University of Technology for the award of the degree of Philosophy, is a bona fied record of the research work done by him under my supervision in the duration of the three years from November 2008 to October 2011. He has completed the work truthfully and successfully to the best of my knowledge. The contents of this thesis, in full or in partial have not been submitted to any other Institute or University for the award of any degree or diploma.

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# Synopsis

Multiple-valued logic, in which the number of discreet logic levels is not confined to two, has been the subject of much research over many years. The practical objective of this work has been to increase the information content of the digital signals in a system to a higher value than that provided by binary operation .To increase the transmission capacity of future communication the present binary system is becoming very critical. A more formal approach would be an n-valued logic which has n different states, each state having a unique identifier. Multi-valued logic (MVL) is defined as a non-binary logic and involves the switching between more than two states. As an example quaternary logic has four logical states viz. 0, 1, 2 and 3. Multi-valued logic can be viewed as an alternative approach to solve many problems in transmission, storage and processing of large amount of information in digital signal processing [1-10]. In the field of data communication, the quaternary codes are preferred because four-valued (i.e. quaternary) logic signals easily interface with the binary world as shown in figure-1. They may be decoded directly into their two binary-digit equivalent. Quaternary logic world can easily be interfaced with binary logic Decoder and Encoder schemes, as $0_4 = (00)_2$, $1_4 = (01)_2$, $2_4 = (10)_2$ and $3_4 = (11)_2$. The block diagram of this interfacing circuit is shown in the figure-1. Of late, renewed interest in optical computing has been witnessed due to the emergence of novel photonics structures that includes nano-photonics, silicon photonics, bio-photonics and plasmonics etc. [11-15]. As photon is the ultimate unit of information with unmatched speed and with data package in a signal of zero mass, the techniques of computing with light may provide a way out of the limitations of computational speed and complexity inherent in electronic computing [15]. In electronics, efforts have already been made to incorporate MVL in logic and arithmetic data processing [3-4, 6]. But, very little efforts have been given in realization of MVL with optics. Polarization properties [16-17] of light can show a light in this regard. Here, in this Ph D thesis, some logic circuits have

been proposed and described to use optics in all-optical quaternary (4-valued) multi-valued system.

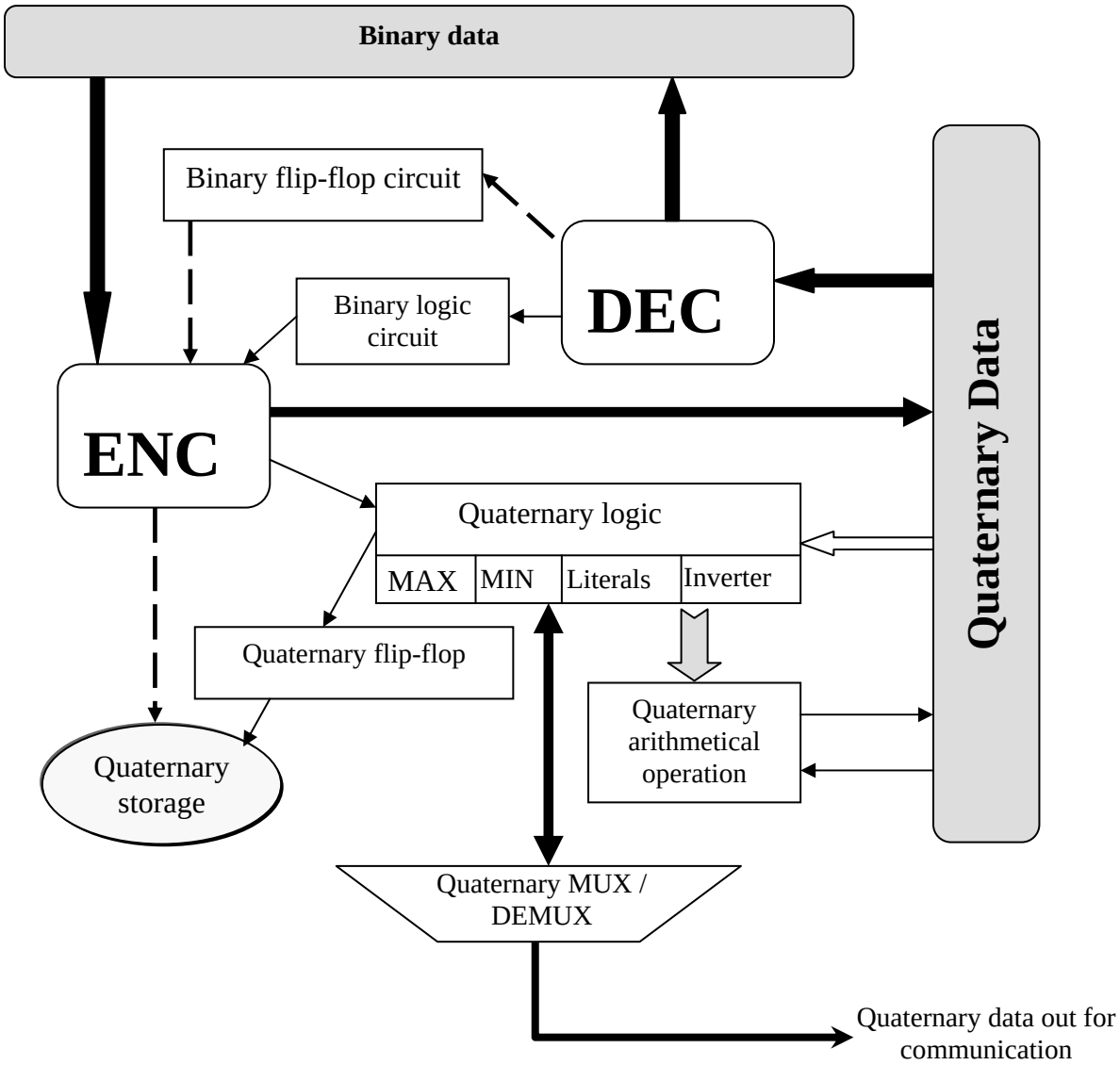



Figure-1: Interfacing Binary and Quaternary world by the help of ENC and DEC.

# Chapter: 1

# Introduction:

The main advantages of multi valued logic systems and circuits are greater speed of arithmetic operations realization, greater density of memorized information, better usage of transmission paths, decreasing of interconnections complexity and interconnections area, decreasing of pin number of integrated circuits and printed boards, possibilities for easier testing [1-5]. In introduction section, a brief review on the prospect and opportunities of multi-valued logic for future generation all-optical computing has been discussed. Special emphasis has been given on quaternary logic based system. Objective and organization of the thesis is given in this chapter.

***Objective of the Thesis:***

The main objective of the thesis is to design different quaternary (4-valued) circuits in all-optical domain with the help of ultra-high speed interferometric switches and exploiting the polarization properties of light. For the quaternary data processing in optics, the quaternary numbers (0, 1, 2, 3) can be represented by four discrete polarized state of light, as shown below:

0 = No light (null)

1 = vertically polarized light ( ↕ )

2 = horizontally polarized light ( • )

3 = partially polarized or Un-polarized light (  )

The content of this Thesis is organized in nine chapters.

- Chapter-1 presents the brief introduction regarding multi-valued system.
- Principle of different ultrafast fiber Interferometric switches like NOLM, TOAD and MZI have been discussed in Chapter -2. Special emphasis has been given to TOAD based switch.
- Chapter-3 deals with designing of some basic quaternary logic gates like QMAX, QMIN, Literals, Successor and Inverter.
- Chapter-4 reports a new polarization encoded all-optical scheme, insensitive to light intensity, for binary to quaternary encoder and quaternary to binary decoder.
- Chapter-5 reports the designing of all-optical circuits for quaternary arithmetic operations like addition and multiplication.
- Simple technique for conversion of *n*-bit binary number (2's compliment form) to quaternary signed digit (QSD) and vice versa is given in Chapter-6. An all-optical circuit is also designed for proposed conversion processes.
- In chapter-7, the principles and possibilities of designing of all-optical quaternary multi-valued multiplexer and de-multiplexer circuits are proposed and described with the help of quaternary min and quaternary delta literal gates.
- Polarization encoded all-optical quaternary (4-valued) R-S Flip-flop with the help of encoder/decoder and one bit binary latch is proposed and described in Chapter-8. The outline of Multi-valued (quaternary) flip-flop using quaternary universal inverter is also given.
- Finally, conclusions and future scope of work is briefed in Chapter-9.

Organization of thesis at a glance is given in Figure-2

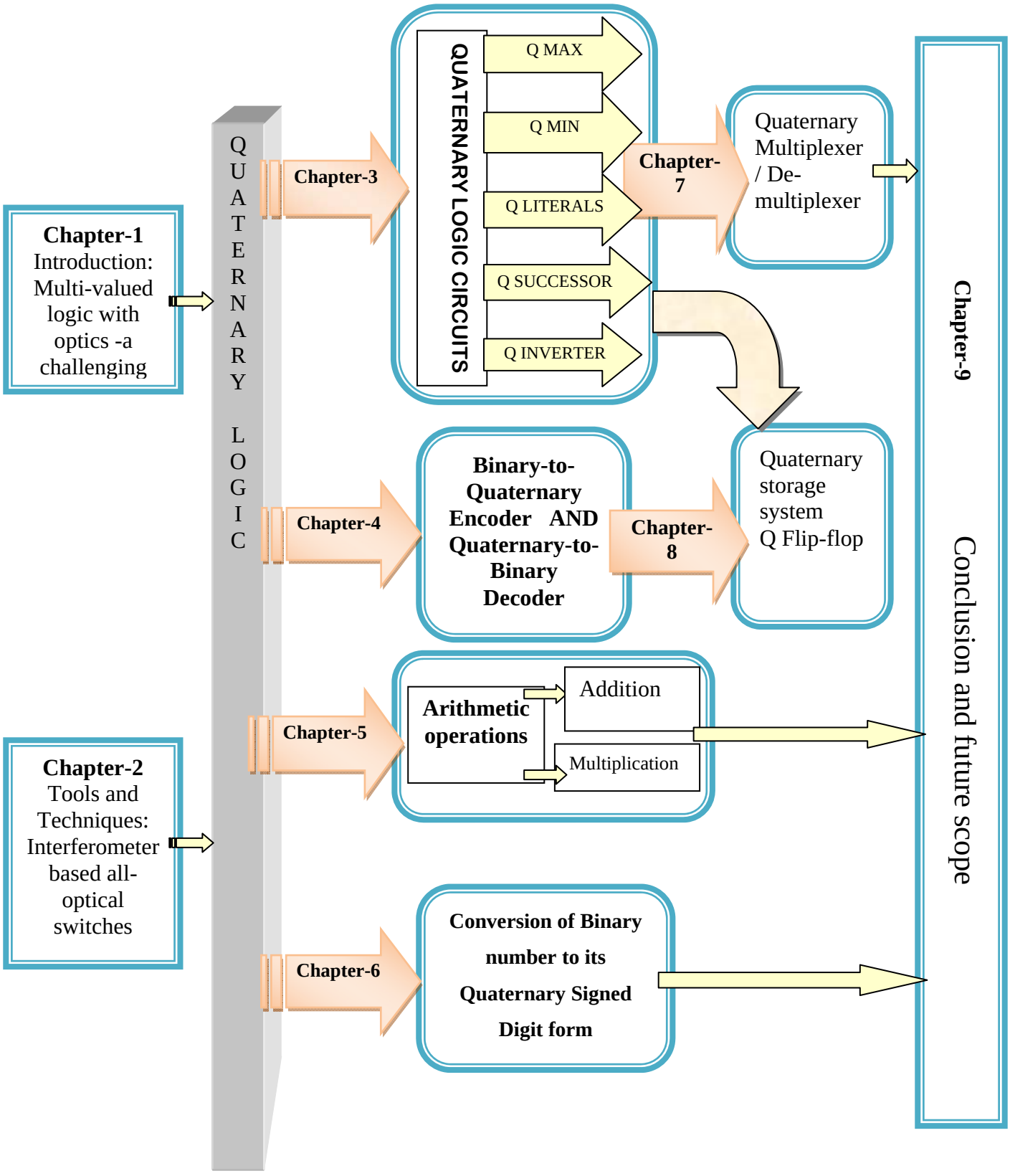



Figure-2: Organization of thesis

# Chapter: 2

## Ultra-fast all-optical fiber-Interferometric switches

The new generation of communication networks is moving towards terabit per second data rates. Such data rates can be achieved if the traditional carrier of information, electron, are replaced by photon for devices based on switching and logic. Researches into this field have also explored new concepts and ideas. By taking the advantage of the nonlinear dynamics in semiconductor optical amplifiers in combination with the fiber interferometers a new generation of ultra-fast all-optical switches have already been reported. A brief overview of different ultra-fast all-optical fiber interferometric switches has been given with an emphasis to terahertz optical asymmetric demultiplexer (TOAD) based switch in this chapter with supporting references. [18-23].

# Chapter-3

## Polarization Encoded All-optical Quaternary Logic Gates

The development of all-optical logic technology is important for a wide range of applications in all-optical networks, including high speed all-optical packet routing, optical encryption and optical computing. An important step in the development of this technology is a demonstration of optical logic elements and circuits, which can also operate at high speeds. Logic gates are basic building block in quaternary logic system. In quaternary logic there are $4^{4^2}$ kinds of functions. The design, principle of operation of polarization encoded all-optical logic gates for some basic quaternary logic operations like QMAX, QMIN, Literals, Successor and Inverter have been

proposed and described in Chapter-3. Gates have been designed with the help of Terahertz Optical Asymmetric Demultiplexer (TOAD) based interferometric switches. Simulation result confirming described method is presented in chapter-3. All-optical quaternary logical gates are shown in Figure-3 below. Also simulated waveform of quaternary MAX, literals, successor, universal inverter (QUI) shown in Figure-4.

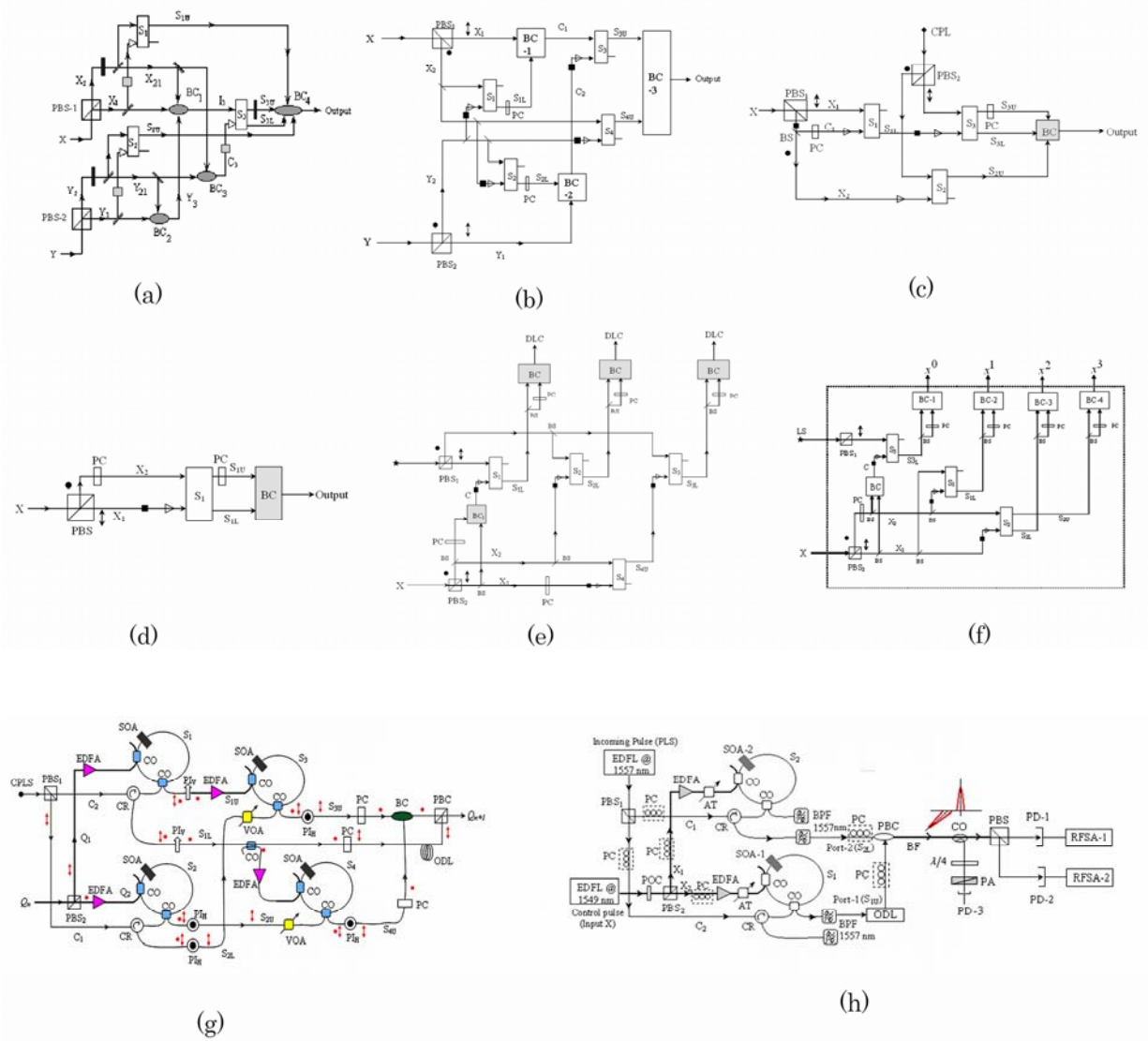



Figure-3: Different all-optical quaternary logic circuits (a) Quaternary MAX gate, (b): quaternary MIN gate, (c) All-optical QTS circuit, (d) All-optical QTD circuit, (e) All-optical Quaternary Down Literal circuits, (f) All-optical Quaternary Delta Literal Circuit, (g) all optical quaternary successor circuit. (h) All optical quaternary universal inverter.

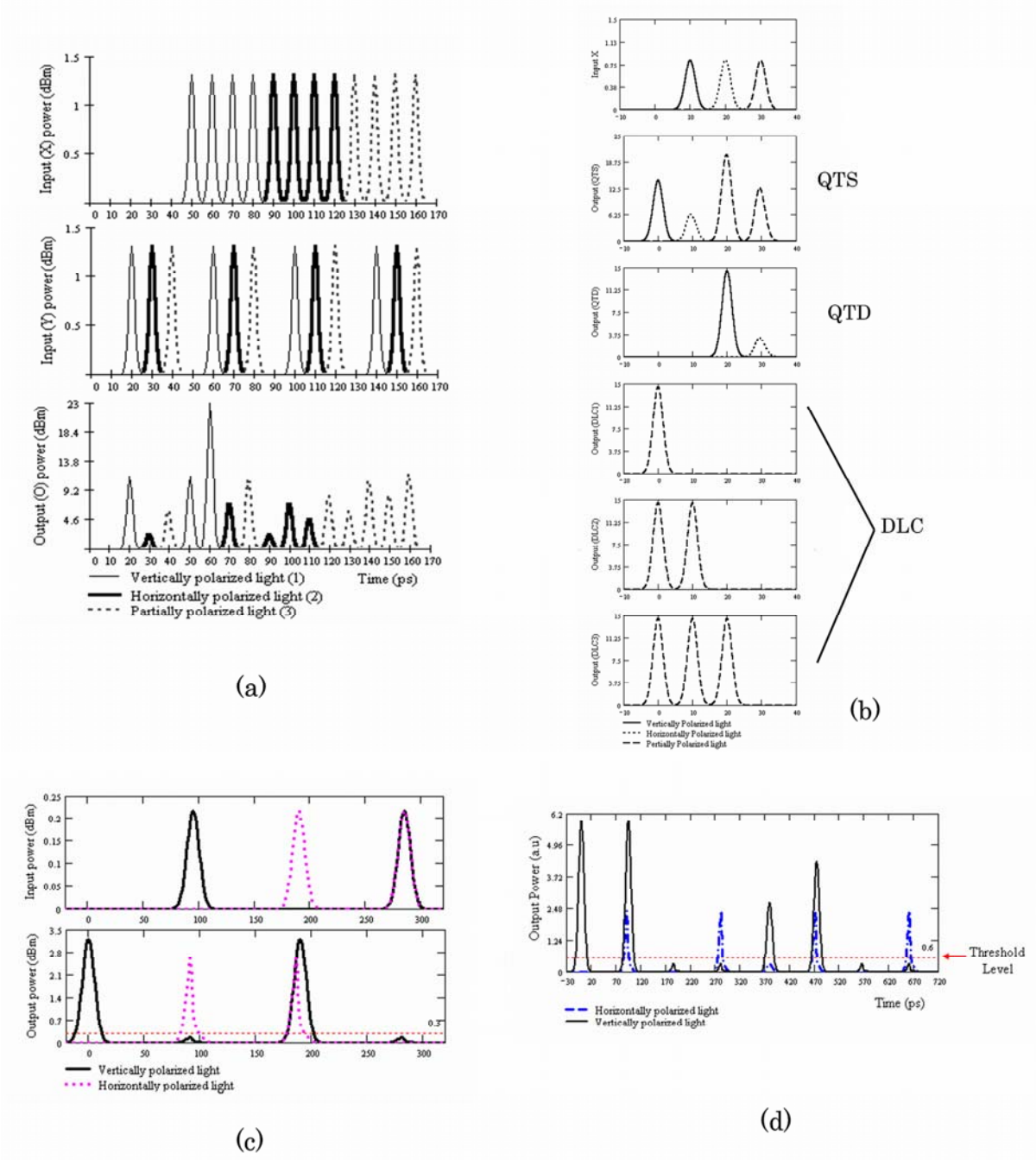



Figure-4: Simulated wove form of the quaternary circuits. (a) MAX, (b) literals, (c) successor, (d) universal inverter (QUI).

The significant advantage of this scheme is that the logical operation, which can be performed, is all-optical in nature. It can be used to build up multi-valued programmable logical array (PLA), memory device (flip-flop), multi-valued counter etc.

# Chapter-4

## Binary-to-quaternary Encoder and Quaternary-to-binary decoder

A simple yet novel all-optical scheme for the conversion of binary to quaternary data and vice versa has been proposed and described in **Chapter-4.** The circuit is numerically simulated and investigated (shown in Figure-5).

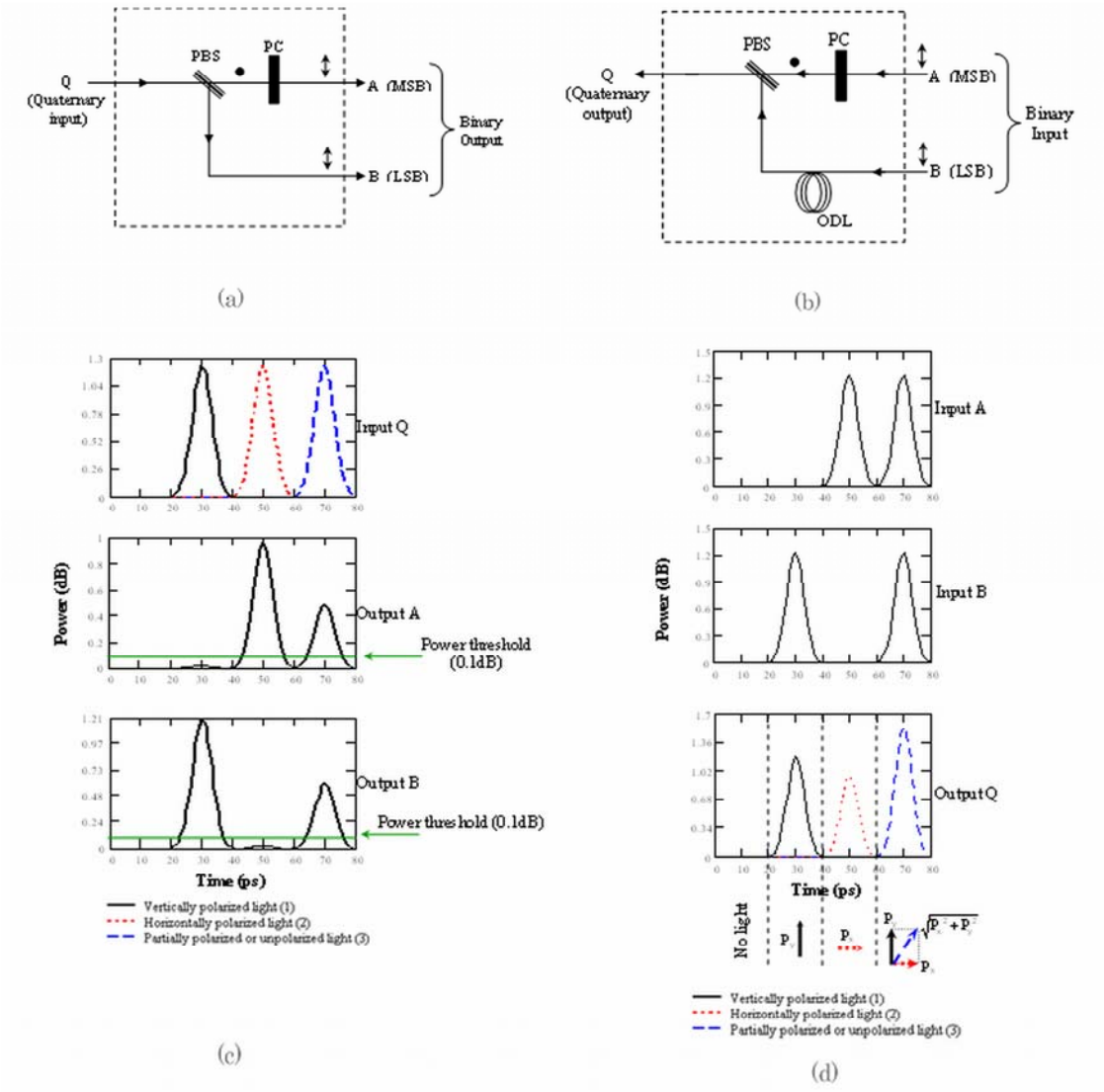



Figure-5: Optical circuit for all-optical quaternary-to-binary decoder (DEC), (b) circuit of all-optical binary-to-quaternary encoder (ENC), (c) wave form of DEC, (d) wave form of ENC.

In this reported all-optical scheme of decoder we have shown that the Contrast Ratio is 13.57 dB and bit error rate is of the order of $10^{-6}$ for both the port. For Encoder unit the value of *SNR* is 14.31 dB and *BER* is of the order of $10^{-13}$ . This scheme is easily practicable as the components of our design are technically highly developed and widely used in optical communication. Proposed DEC/ENC scheme will be helpful in designing GF(4) adder and multi-valued memory cell.

# Chapter-5

## All-optical quaternary arithmetic Operations

Multiple valued logic functions having many input variables can easily be expressed as Galois field sum of product (GFSOP) expression. **Chapter-5** reports the designing of GF(4) arithmetical circuit and QGFSOP circuit. The principle and possibilities of all-optical GF(4) adder circuit (shown in Figure-6) is described and theoretical model is presented and verified through numerical simulation .The principle of operation and all-optical circuits for GF(4) multiplication is also presented in this chapter. Some probable application of all-optical Quaternary Galois field GF(4) adder and sum of product (QGSOP) are also mentioned.

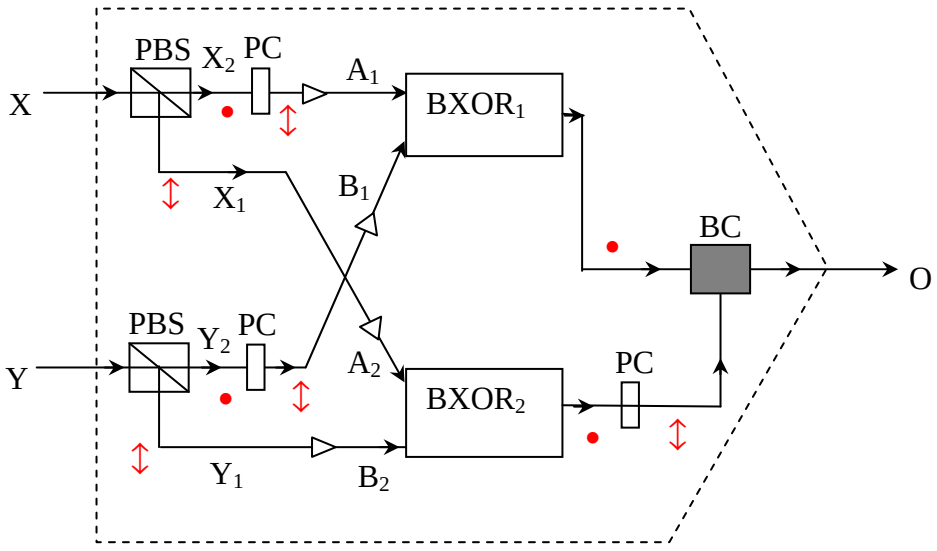



Figure-6: All-optical GF (4) adder circuit**:** EDFA: $Er^{+3}$ doped fiber amplifier, BC: Polarization beam combiner, PC: Polarization controller, BXOR: Binary XOR gate.

# Chapter-6

## Conversion of Binary number to its Quaternary Signed Digit form

**Chapter-6** reports a new and easy method for conversion from binary number (2's compliment representation) to its quaternary signed digit (QSD) form and conversion of QSD to its binary equivalent form. Tree structure based all-optical circuit (shown in Figure-7) is presented along with the numerical simulation. This conversion technique is extended for higher digit. New conversion technique for *n*-bit binary to *m*-digit QSD and vice versa is presented with some examples. This conversion scheme can be implemented in all-optical domain. Outline of its optical implementation is also proposed.

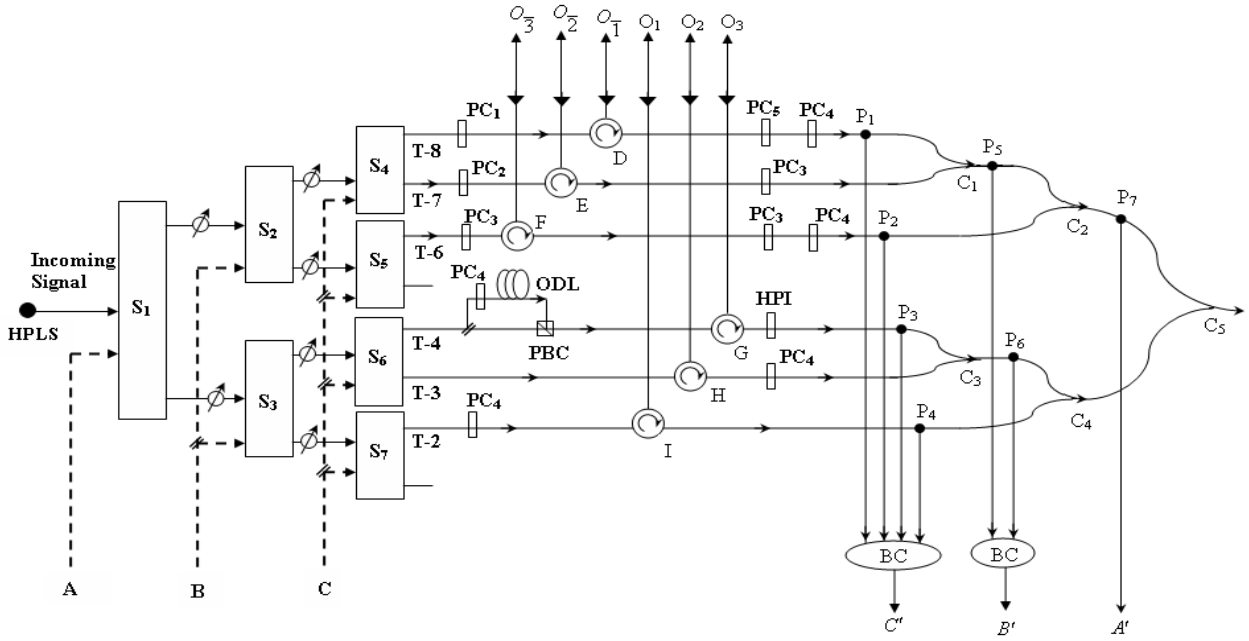
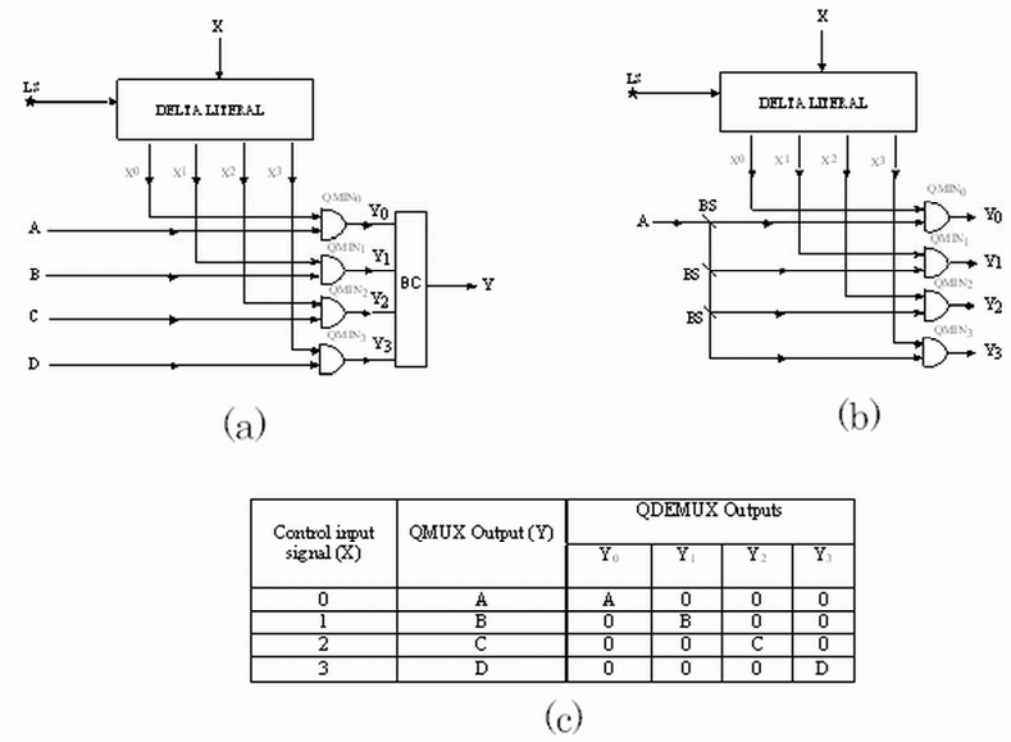



Figure-7: All-optical encoder-decoder (ENC-DEC) blocks (binary-to-QSD encoder and QSD-to-binary decoder). : Beam splitter, PBC: polarization beam combiner, PC: polarization converter, BC: beam combiner, ODL: 5 ps optical delay line. For binary-to-QSD encoder circuit inputs are A, B and C. Outputs are $O_1$, $O_2$, $O_3$, $O_{\bar{3}}$, $O_{\bar{2}}$ and $O_{\bar{1}}$. For QSD-to-binary decoder inputs are $O_1$, $O_2$, $O_3$, $O_{\bar{3}}$, $O_{\bar{2}}$ and $O_{\bar{1}}$. Outputs are $A'$, $B'$ and $C'$.

# Chapter-7

## Polarization Encoded All-optical Quaternary multiplexer / De-multiplexer

Multiplexing and de-multiplexing are two essential features in almost all the signal communication systems, where a lot of information is being handled without any mutual disturbances. In **chapter-7**, the principles and possibilities of designing of all-optical quaternary multi-valued multiplexer and de-multiplexer circuits are proposed and described with the help of quaternary min and quaternary delta literal gates (shown in Figure-8).




| Control input signal (X) | QMUX Output (Y) | QDEMUX Outputs | | | |
|---|---|---|---|---|---|
| | | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ |
| 0 | A | A | 0 | 0 | 0 |
| 1 | B | 0 | B | 0 | 0 |
| 2 | C | 0 | 0 | C | 0 |
| 3 | D | 0 | 0 | 0 | D |

(c)

Figure-8: All optical circuit for (a) quaternary Mutimplexer (b) quaternary demultiplexer, (c) truth table**.**

# Chapter-8

## Polarization encoded all-optical Quaternary R-S Flip-flop

The memory device is very important in photonic information processing as they store various values either temporary or permanently. Two different all-optical circuits, one using encoder-decoder (shown in Figure-9) and other using quaternary universal inverter circuit, have been proposed and described for designing of the quaternary RS flip-flop in **Chapter-8**. Polarization properties of light have been exploited in this regard. Here, the binary latch has been used to build the quaternary memory unit.

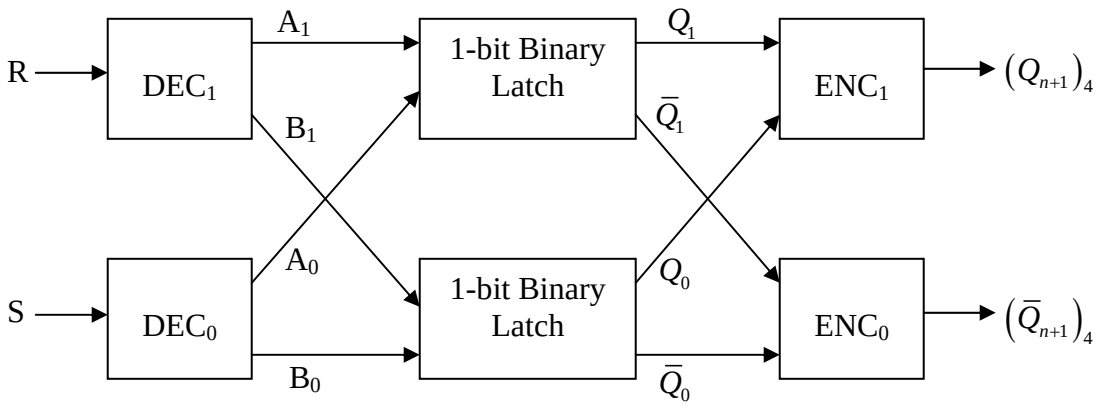



Figure-9: Quaternary memory unit (R-S flip-flop).

Simulation result (by Mathcad-7.0) confirming described methods is given in this paper. Insertion losses, extinction ratios have been calculated for quaternary (4-valued) R-S Flip-flop circuit designed with all-optical encoder/decoder and a binary latch. Outline of Multi-valued (quaternary) flip-flop using quaternary universal inverter is also given.Logical simulation is done.

# Chapter: 9

## Conclusion and future scope of work

**Conclusion:**

In this Thesis different MVL circuits have been designed in all-optical domain with the help of ultra-high speed interferometric switches and exploiting the polarization properties of light**.** In most of the cases, theoretical model has been established. Numerical simulation results (by Mathcad-7.0) confirming described method have been presented. Detail discussions (like measurement of extinction ratio, insertion loss, degree of polarization of the output for different control pulse energy, bit error rate etc) have been done for proposed polarization encoded all-optical quaternary logic circuits it. To make the simulation more realistic the data have been taken from a published literature that reports experimental results. The theoretical models developed and the results obtained numerically are useful to future all-optical logic based information processing system. The significant advantage of this scheme is that the operations are all-optical in nature. Our reported schemes are expected to be also valid for other 2x2 interferometric switches based on SOA and thus might be fruitful for optical computing devices in near future.

**Future Scope:**

In this Thesis we tried to give a basic idea and circuits of all-optical basic quaternary logic and information processing scheme that may helps to build quaternary optical computer (QOC) in future. To build QOC we have to synchronize all the logic gates in a

proper way such that it can perform an operation well. The future scope of quaternary logic based signal processing some interesting work can be done, which is shown below (Figure-10).

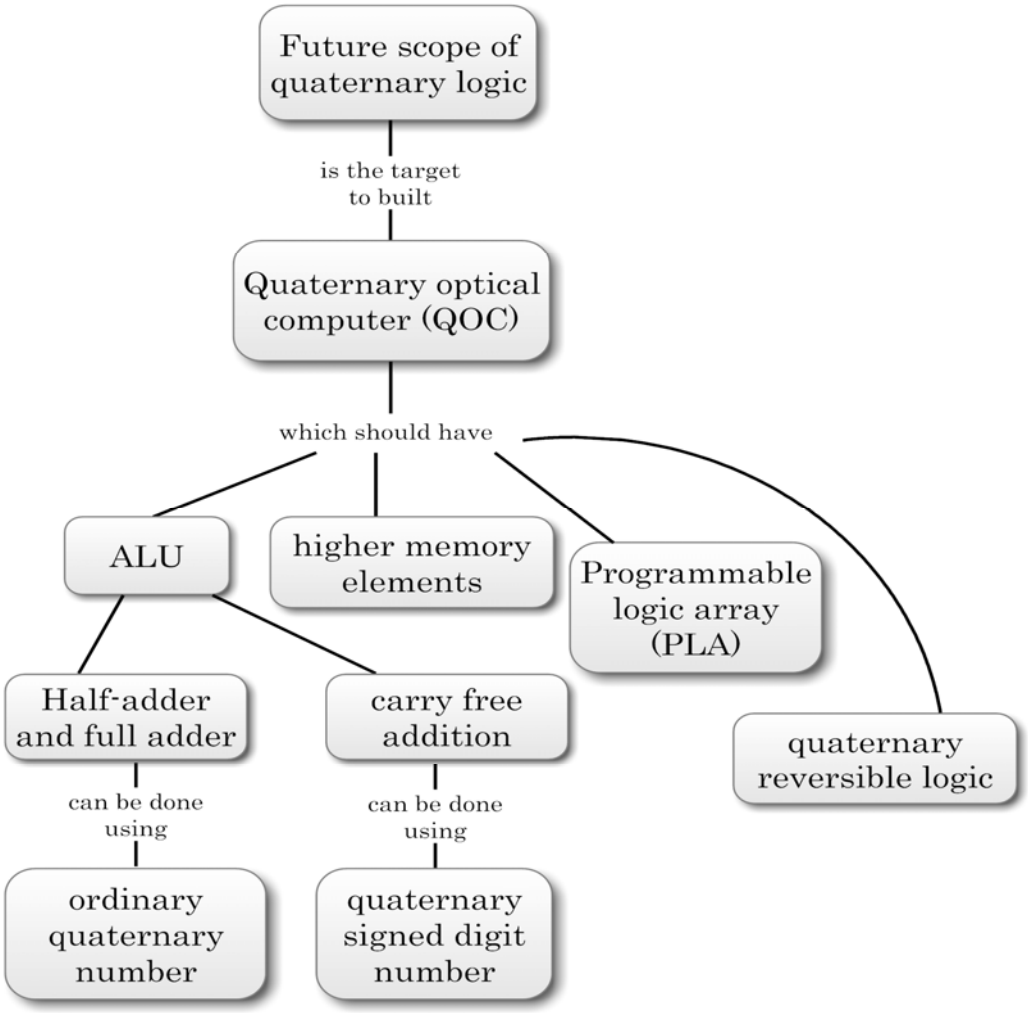



Figure-10: Future scope of all-optical quaternary signal processing

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# List of published /accepted/communicated papers related to PhD Thesis

## International Referred Journal:

1. **T.Chattopadhyay** and J.N.Roy, "Polarization encoded all-optical quaternary successor with the help of SOA assisted Sagnac switch", *Optics communication*, (Elsevier), 284(12), (2011), 2755-2762.
2. **T.Chattopadhyay** and J.N.Roy, "All-optical quaternary Galois field sum of product (GFSOP) circuits", *Optik International Journal for Light and Electron Optics*, (Elsevier), 122(9), (2011), 758-763.
3. **T.Chattopadhyay**, M.K.Das, J.N.Roy, A.K.Chakraborty and D.K.Gayen, "Interferometric switch based all optical scheme for Conversion of Binary number to its Quaternary Signed Digit form", *IET Circuits, Devices and system*, (**special issue on 'Optical Computing Circuits, Devices and Systems'**), 5(2), (2011), 132-142. (**Cited by-1**)
4. **T.Chattopadhyay** and J.N.Roy, "Easy conversion technique of Binary to Quaternary Signed Digit and vice versa", *Physics Express*, (Simplex-academic-publishers), 1(3), (2011), 165-174.
5. **T. Chattopadhyay** and J. N. Roy, Polarization encoded TOAD based all-optical quaternary Literals, *Optik International Journal for Light and Electron Optics*, (Elsevier), 121, (2010), 617-622.
6. **T.Chattopadhyay** and J.N.Roy, "Polarization Encoded All-optical Quaternary Universal Inverter and Designing of Multi-valued Flip-flop", *Optical Engineering*, (SPIE). 49(3), 035201 (2010), doi: 10.1117/1.3362897.
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8. **T.Chattopadhyay**, J.N.Roy and A.K.Chakraborty, "Polarization encoded all-optical

quaternary R-S flip-flop using binary latch", *Optics Communications*, (Elsevier), 282, 1287-1293 (2009). (**Cited by-4**)

9. **T.Chattopadhyay** and J.N.Roy, "An all-optical technique for a binary-to-quaternary encoder and a quaternary-to-binary decoder", *J.Opt.A: Pure Appl. Opt.* (IOP), 11 (2009) 075501 (8pp) doi:10.1088/1464-4258/11/7/075501.

## Conferences and proceedings:

10. **T.Chattopadhyay** and J.N.Roy, "All-optical multi-valued computing: the future challenges and opportunities", *International conference on convergence of Optics and Electronics*, (COE 11), March 26-27, 2011, Kolkata, pp. 94-101, ISBN 978-81-906401-1-4.
11. **T.Chattopadhyay** and J.N.Roy, "All-optical carry free addition using quaternary signed digit (QSD)", *18$^{th}$ West Bengal state science & Technology congress*, 28$^{th}$ February- 1$^{st}$ March 2011, 1PP(2), 3-4.
12. **T.Chattopadhyay** and J.N.Roy, "All-optical quaternary half-adder circuit with the help of Terahertz optical asymmetric demultiplexer (TOAD)", National conference on materials, devices and circuits in communication Tech. (*MDCCT'2010*), 27-28 March, Burdwan, TS. 4.12, pp-50.
13. **T.Chattopadhyay** and J.N.Roy, "All-optical conversion of binary number to quaternary signed digit (QSD) number", *Proceedings of international conference on Trends in optics and photonics (IconTOP 2009)*, March 1-4, 2009, Kolkata, India, 130-137, ISBN 978-81-908188-0-3.
14. J.N.Roy, **T.Chattopadhyay**, S.Manna and G.K.Maity, "Polarization encoded all-optical quaternary max gate", *PHOTONICS-2008*: International Conference on Fiber Optics and Photonics, December 13-17, 2008, pp-1-4, IIT Delhi, India.
15. **T.Chattopadhyay** and J.N.Roy, "Polarization encoded four valued ordinary inverter", *XXXVI OSI Symposium on Frontiers in Optics and Photonics*, (FOP 11), (Accepted).